IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Wilbur Catabay
Richard Schinella

Serial No. :	10/099,641	**Group Art Unit :**	2829
Filed :	March 15, 2002	**Examiner :**	Kilday, Lisa
For :	Low K Dielectric Composite Layer for Integrated Circuit Structure Which Provides Void-Free Low K Dielectric Material Between Metal Lines While Mitigating Via Poisoning	**Atty Docket :**	/ 99-102/1D

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Connie Del Castillo

8/09/04 Connie del Castillo

Date Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll

Reg. No. 36,771

Date: 4 Aug 04